REMARKS

I. Status of the Application

Claims 9-28 are pending in this application. In the August 8, 2007 Office action, the Examiner:

A. Objected to claims to 9-28 as allegedly including informalities;

B. Rejected claims 9, 11, 13, 14, 16, 18, 20, 21, 23, 25 and 26 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent no. 5,210,828 to Bolan et al. (hereinafter "Bolan");

C. Rejected claims 10, 17 and 22 under 35 U.S.C. § 103(a) as allegedly being obvious over Bolan in view of U.S. Patent No. 4,935,894 to Ternes et al. (hereinafter "Ternes"); and

D. Rejected claims 12, 15, 19, 24, 27 and 28 under 35 U.S.C. § 103(a) as allegedly being obvious over Bolan.

In this response, Applicant has amended claims 9, 16, 21 and 26 to clarify the claimed subject matter. As set forth below, Applicant respectfully traverses the Examiner's rejection of claims 9-28.

II. The Objections to the Claims

The Examiner objected to the claims for informalities, and suggested amendments to claims 9, 16, 21 and 26 to address the informalities. Applicants have amended claims 9, 16, 21 and 26 substantially as suggested by the Examiner. It is therefore respectfully submitted that the objections to the claims are moot and should be withdrawn.

III.   The Rejection Under 35 U.S.C. 102 (b) Should be Withdrawn

To establish a *prima facie* case of anticipation, the Examiner must show that

each and every element as set forth in the claim is found either expressly or inherently

in a single prior art reference M.P.E.P. §2131.

In the August 8, 2007 office action, the Examiner rejected claims 9, 11, 13, 14,

16, 18, 20, 21, 23, 25 and 26 under 35 U.S.C. § 102(b) as allegedly being anticipated

by Bolan. Applicant respectfully traverses these rejections. Applicant submits that

each and every element as set forth in claims 9,11,13,14,16,18,20,21,23,25 and 26 is

not found, either expressly or inherently, in Bolan. Thus, the cited reference does not

anticipate the claimed invention. Claims 9, 21 and 26 are to be amended to add further

limitations not found in Bolan. In view of these amendments, the rejection over Bolan

is moot.

Claims 9, 21 and 26 now require, *inter alia*:

> Storing at least a first data packet of the first message in the ancillary memory
> without storing the first data packet in the main memory

In contrast Bolan teaches holding registers 61-63, which the Examiner has

interpreted as a main memory, each of which receive the entire message to be

transferred to the receiving processor. This corresponds to the prior art described at

pages 1 and 2 and shown in Figure 1 of the present application. Accordingly Bolan

teaches directly away from storing the first data packet in the ancillary memory

without storing the first data packet in the main memory.

The Examiner states at paragraph number 3 page 3 of the August 8, 2007

office action that "segmentation is inherent for large message size depending on the

bus transferring capacity". The Applicant disagrees with this interpretation. There is

no evidence that Bolan is configured to receive messages of a large message size that
would require message segmentation.

Claims 9, 21 and 26 now also require, *inter alia*:

Transferring at least one other stored data packet of the first message to the
ancillary memory from the main memory

The Examiner states at paragraph 3, page 4 of the August 8, 2007 office action
that Bolan discloses a "message is retrieved from the addressed mailbox entry and
placed in the message output register". However claims 9, 21 and 26 require that the
replenishment of the ancillary memory is in relation to other data packages of a
specific message. Bolan does not disclose that the ancillary memory is replenished by
the main memory with other data packets of a particular message. Also since the
Examiner has collectively interpreted the mailbox array 105 *and* the message output
register 160 as an ancillary memory, it is not clear how transferring a message
between the mailbox array 105 and the message output register 160 could constitute
replenishing the ancillary memory from the main memory. Such a transfer would be
from the ancillary memory to the ancillary memory.

Therefore Bolan does not disclose at least:

1. the first data packet only being stored in the ancillary memory,

2. segmentation of the message, and

3. replenishing the ancillary memory with other data packets of a specific
   message from the main memory.

Because Bolan fails to teach the required elements of claim 9, 21 or 26, it is
respectfully submitted that claims 9, 21 and 26 are all allowable over the prior art of
record.

Claims 11, 13, 14, depend from claim 9 and claims 23, 25 depend from claim

21 and add further limitations thereto. As discussed above, Bolan fails to teach each and every element of claims 9 and 21. Accordingly, it is respectfully submitted that the dependent claims 11, 13, 14, 23 and 25 are allowable by reason of depending from an allowable claim as well as for adding new limitations.

IV.   The Rejections Under 35 U.S.C. § 103(a) Should Be Withdrawn

In the August 8, 2007 Office action, the examiner rejected claims 10, 12, 15, 17, 19, 22, 24, 27 and 28 under 35 U.S.C. § 103(a) as allegedly being obvious and unpatentable over Bolan and Ternes or Bolan individually. Applicant respectfully traverse the examiner's rejection of claims 10, 12, 15, 17, 19, 22, 24, 27 and 28 under 35 U.S.C. § 103(a), as the examiner has not made a *prima facie* case of obviousness as described in MPEP § 2142 - 2143. In view of the amendment to claims 9, 21 and 26 these objections are now moot.

A.   Claims 10,17 and 22

In order for the examiner to make a *prima facie* case of obviousness under MPEP § 2143.03, all claim limitations must be taught or suggested by the prior art. In the present case applicant respectfully submits that the examiner has not established a *prima facie* case of obviousness, as all limitations of claims 10, 17 and 21 are not taught or suggested by the prior art. For example neither Bolan nor Ternes teach or suggest:

1.   the first data packet only being stored in the ancillary memory,

2.   segmentation of the message, and

3.   replenishing the ancillary memory with other data packets of a specific message from the main memory.

Accordingly, neither Bolan nor Ternes, teach all the limitations of claim 9 individually or in combination. In similar fashion, neither Bolan nor Ternes teach all the limitations of claim 21 individually or in combination. Applicant does not agree that Bolan or Ternes teach the limitations added by any of these dependant claims. For at least the reason of depending on an allowable independent claim, and for adding additional inventive limitations, claims 10, 17 and 21 are allowable.

Additional reasons also exist for the allowance of claims 10, 17 and 22. To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to a reader of ordinary skill in the art, as of the date of invention, to modify the reference or to combine the reference teachings. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990), or unless the modification is based on common sense, *KSR INT'L CO. v. TELEFLEX INC*, 550 U. S. ____ (2007). Second there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable chance of success must both be found in the prior art, not in the applicant's disclosure. *In re Vaeck*, 947 F.2d 488,20 USPQ2d 1438 (Fed. Cir. 1991). M.P.E.P. § 2143

For example, there is no suggestion or motivation in the art for combining the references. The Examiner states at paragraph 5 page 7 that the motivation to combine Bolan and Ternes is "in order to process multiple packets in sequence between two processors". Firstly, Bolan would not work if the mailbox array 105 and the message output register 160 were replaced with the FIFO register stack 55, 60 of Ternes. Secondly, there is no suggestion in Bolan that packets would not be processed in

sequence and therefore one of ordinary skill in the art would not realize Bolan required improvement. Thirdly, the FIFO register stack 55, 60 in Ternes is not an ancillary memory connected to a main memory and one of ordinary skill in the art would not see Ternes as relevant to Bolan. Fourthly, the alleged motivation does not address the invention 10, 17 and 22. Furthermore, there is no reasonable expectation of success. Accordingly, claims 10, 17 and 22 are allowable for these reasons as well.

B.   Claims 12,15,19,24,27 and 28

In the August 8, 2007 Office action, the examiner rejected dependent Claims 12, 15, 19, 24, 27 and 28 under 35 U.S.C. § 103(a) as allegedly being obvious over Bolan.

Claims 12 and 15 depend from claim 9, claim 24 depends from claim 21 and claims 27 and 28 depend from claim 26. Bolan does not disclose the required limitations of claims 9, 21 or 26. Also, Applicant does not agree that Bolan teaches the limitations added by any of these dependant claims. For example if Bolan does teach four clock cycles to decode and execute a command, as alleged by the Examiner, then the Examiner has clearly shown that Bolan teaches directly away from claim 12. For at least the reasons of depending on an allowable independent claim, and for adding additional inventive limitations, claims 12, 15, 19, 24, 27 and 28 are allowable.

V.   Conclusion

For all of the foregoing reasons, it is respectfully submitted that applicant have made a patentable contribution to the art. Favorable reconsideration and allowance of this application, including claims 9-28, is therefore respectfully requested.